MT6605

Chip spec

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Specifications are in draft stage and subject to change without notice.

Document Revision History

Revision	Date	Author	Description
0.1	2012-09-07	Chun-Yi Wu	Initial Draft
0.2	2012-09-20	Chun-Yi Wu / Wee Liang Lien	Add pin definition
0.3	2012-09-23	Chee Lee Heng / Mark Choke / Wee Liang Lien	Added sections related to RX, TX and SX
0.4	2012-09-24	Chun-Yi Wu	Update chip diagram, feature section

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1 Top Level Overview

1.1 General description

The MediaTek® MT6605 single chip SoC provides full range of 13.56MHz contactless protocols, small footprint, optimized RF performance and power management for variety of NFC applications on mobile, computing and consumer electronics. MT6605 is compliant to NFC Forum, EMVCo, ISO 10373-6, ETSI SWP/HCI and China domestic standards and has been tested with ecosystem key players and infrastructure to ensure interoperability. With highly integrated with MediaTek® platform, MT6605 total solution can save design cost, shorten time-to-market and easily customize for differentiation.

MT6605 has 2 unique designs to enable NFC market eco-system. For payment, it can support up to 2 UICC and 1 Micro SD or Embedded Secure Element through the Single-Wire Protocol (SWP) interfaces. For No-payment, its pre-installed application Beam Plus helps the user to easily tap and share information 2 times faster by optimized WiFi, BT and NFC connection handover.

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1.2 Features

- Reader Features(106K-848Kbits/s)
  - Support ISO 15693
  - Support ISO 14443A
  - Support ISO 14443B, B’
  - Support ISO 18000-3
  - Support NFC Forum Type1-4 Tag
  - Support Kovio
- Card Emulation Mode(106K-848Kbits/s)
  - Support ISO 14443A
  - Support ISO 14443B, B’
  - Support NFC Forum Type1-4 Tag
  - Support Mifare via CLT
  - Support FeliCa RF
- Near Field Communication(106K-424Kbits/s)
  - Peer to Peer Active/Passive mode
  - ISO18092 compliant
- Reference oscillator
  - Internal 27.12 MHz oscillator to support single pin crystal connection
  - Integrated Frac-N PLL which supports multiple external reference clock frequencies of 19.2, 20, 24, 26, 27.12, 38.4, 40 & 52 MHz
  - Co-clock on MediaTek platform
- Processor
  - 16 bits CPU Core
  - NVM independent power domain
  - RAM:48KB, ROM:75.75KB, NVM: 17.5K
- Serial interface
  - UART: 4800bps~921600bps
  - SPI: 2Mbps
  - I2C: Fast mode (400Kbps) / High Speed Mode (3.4 Mbps)
  - SWP : 1.69Mbps (Release 9.2.0)
- Compliance
  - NFC Forum Wave 1 and Wave 2
  - EMVCo 2.0.1 PICC and PCD
  - Visa Paywave and MasterCard Paypass
  - China UnionPay QuickPass
  - ISO 10373-6
  - ETSI/SCP SWP and HCI
  - GSMA
- Package (QFN32)
  - 4mm x 4mm x 0.8mm
  - 4.5mm x 4.5mm x 0.8mm (with embed secure element)

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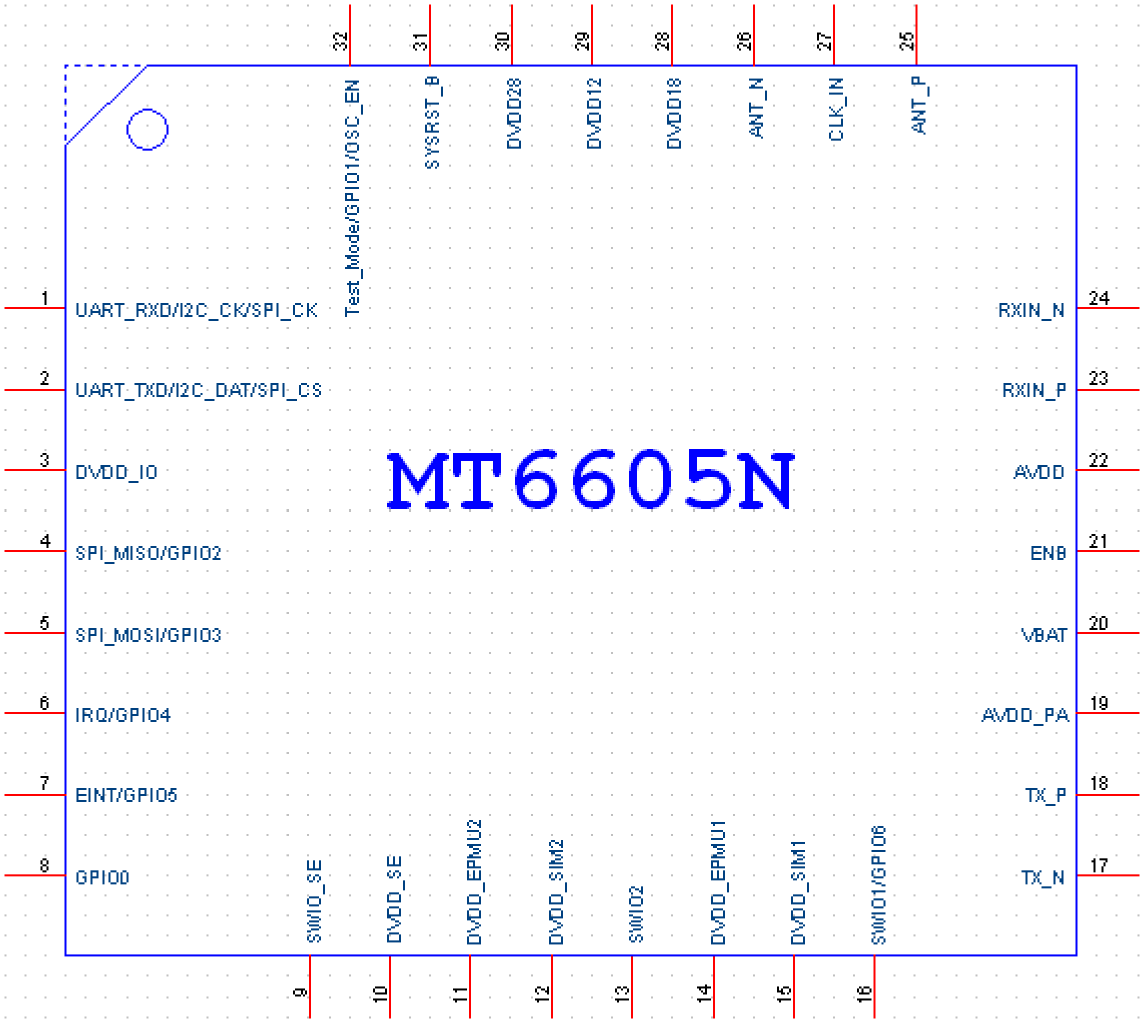
2 Pin Assignment and Descriptions

2.1 Pin assignment (top view)

2.1.1 4 mm x 4 mm



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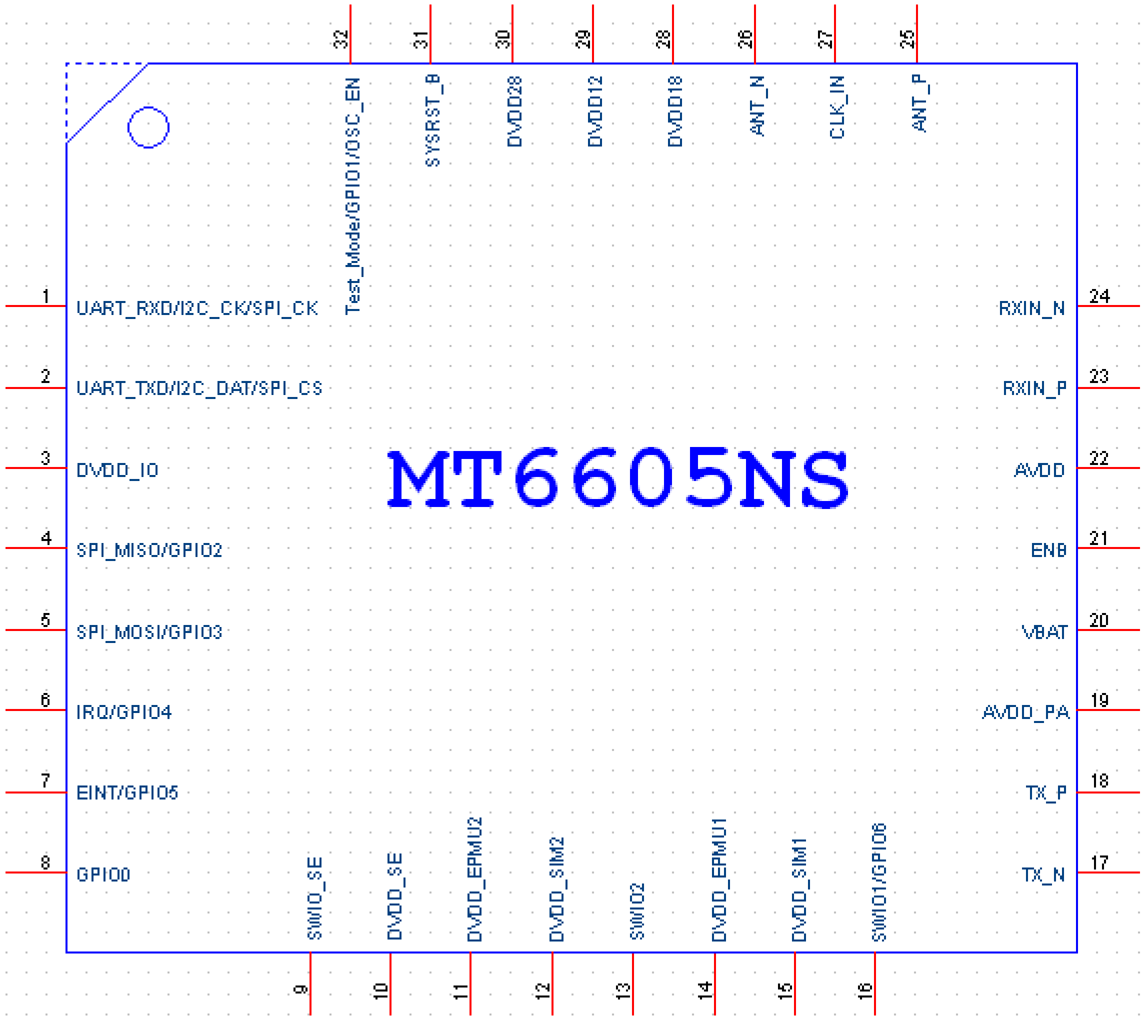
2.1.2 4.5 mm x 4.5 mm



2.2 Pin descriptions

Pin#	Name	Type	Description
Digital Peripheral interface (4 pins)			
1	UART_RXD/I2C_CK/SPI_CK	I/O	Serial input for UART/I2C_CK/SPI_CK Default: pull-up Default: 2mA driving
2	UART_TXD/I2C_DAT/SPI_CS	I/O	Serial output for UART/I2C_DAT/SPI_CS Default: pull-up Default: 2mA driving
4	SPI_MISO/GPIO2	I/O	Serial output for SPI_Data Default: pull-down Default: 2mA driving Strap pin : eclk_sel
5	SPI_MOSI/GPIO3	I/O	Serial input for SPI_Data Default: pull-down Default: 2mA driving

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Digital system interface (5 pins)			
21	ENB	I/O	System enable. Active low
31	SYSRST_B	input	System reset. Active low Default: pull-up
32	TEST_MODE/GPIO1/OSC_EN	I/O	Test mode enable/GPIO1/OSC_EN 1: test mode. 0: normal mode. Default: pull-down Strap pin osc_en
6	IRQ/GPIO4	I/O	TX request indicator/GPIO4 Default: pull-down Default: 2mA driving Strap pin: host_sel[1]
7	EINT/GPIO5	I/O	External interrupt Default: pull-down Default: 2mA driving
Digital debug interface (1 pins)			
8	GPIO0	I/O	GPIO Default: pull-down Default: 2mA driving Strap pin: host_sel[0]
SWP			
9	SWIO_SE	I/O	SWP IO for SE/microSD
13	SWIO2	I/O	SWP IO 2
16	SWIO1/GPIO6	I/O	SWIO IO 1
PMU			
3	DVDD_IO	Power input	External host VDD (2.8v/1.8v)
10	DVDD_SE	Power output	Output VDD for microSD, eSE (1.8v)
11	DVDD_EPMU2	Power input	External PMU2 VDD (3v/1.8v)
12	DVDD_SIM2	Power output	Output VDD for SIM2 (1.8v)
14	DVDD_EPMU1	Power input	External PMU1 VDD (3v/1.8v)
15	DVDD_SIM1	Power output	Output VDD for SIM1 (1.8v)
19	AVDD_PA	Power output	LDO output for LDO PA
20	VBAT	Power input	Battery voltage (4.3v)
22	AVDD	Power output	Rectifier output (2.6v)
28	DVDD18	Power output	Secure element power supply output (1.8v)
29	DVDD12	Power output	Baseband power supply output (1.2v)
30	DVDD28	Power input	LDO input for SRAM data retention (2.8v)
RF & analog			
17	TX_N	Analog output	Transmitter output negative terminal
18	TX_P	Analog output	Transmitter output positive terminal
23	RX_IN_P	Analog input	Receiver input positive terminal
24	RX_IN_N	Analog input	Receiver input negative terminal (optional)
25	ANT_P	Analog input	Rectifier input positive terminal
26	ANT_N	Analog input	Rectifier input negative terminal

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27	CLK_IN	Digital input	27.12MHz XO input or co-clock

2.3 Strap function

TEST_MODE	SPI_MISO	IRQ	GPIO0	Function
	eclk_sel	host_sel[1]	host_sel[0]	
0		0	1	UART without buad detect (TCXO 27.12M/115200)
0		1	0	UART with buad detect
0		0	0	I2C
0		1	1	SPI
0	0			Use self clock
0	1			Co-clock (26M)

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3 Block Diagrams

3.1 Chip overall block diagram

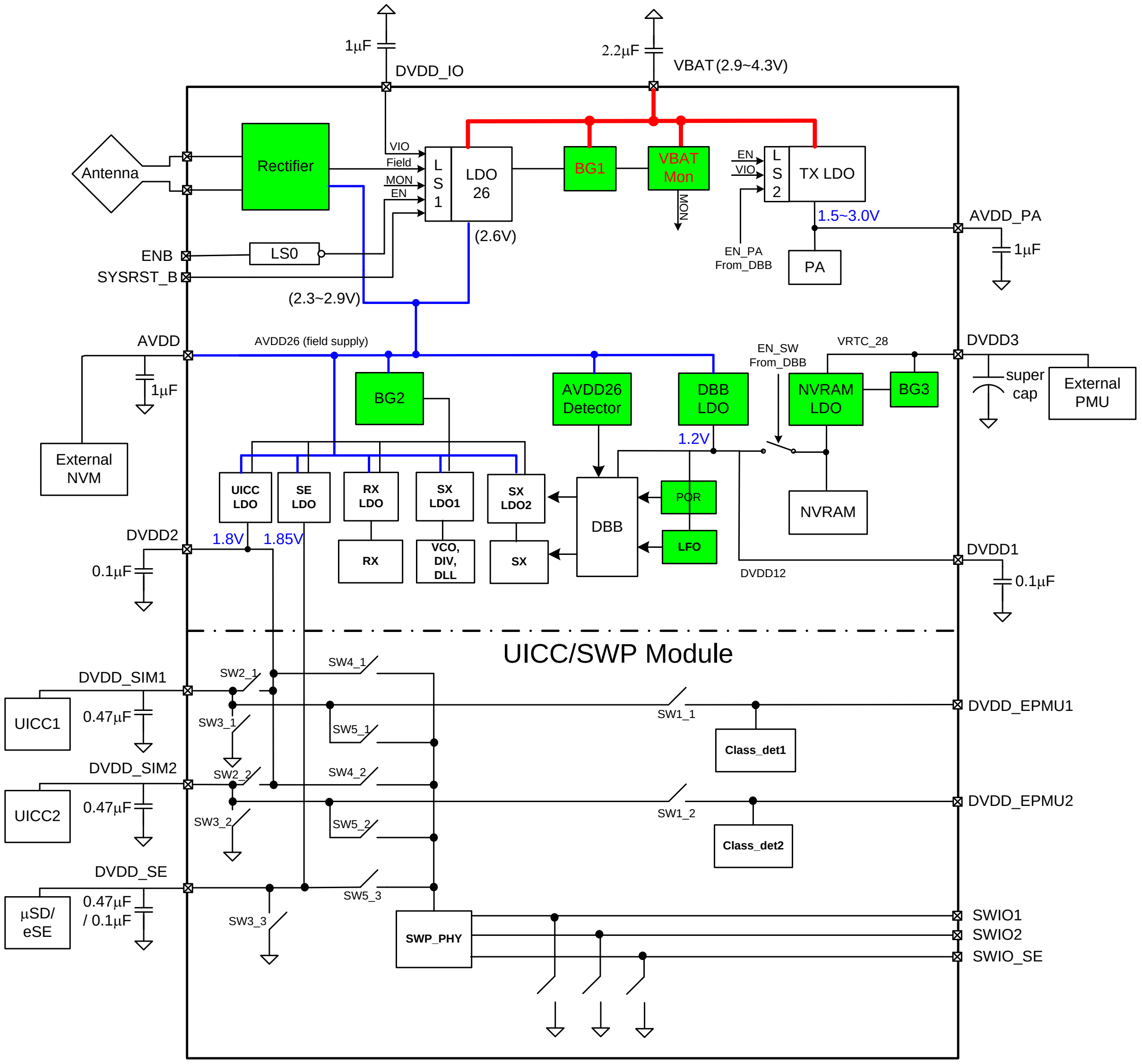

Figure 3-1: MT6605 functional blocks

The block diagram of MT6605 is illustrated in Figure 3-2. MT6605 comprises of 7 main blocks: RX, TX, SX, SWP, Baseband, power harvester and the power management unit (PMU).

This direct conversion RX directly translates the received PCD or PICC signal to base-band frequencies for digital demodulation.

The TX section has a high efficiency PA to provide modulated signals during the PCD mode.

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In the SX section, the Low Frequency Oscillator (LFO) will be enabled when AVDD26 is available. The LFO generates 300KHz clock to DBB and is the main clock source during sleep and low power polling. A frac-N PLL generates 13.56MHz clock for RF field generation and DBB during PCD mode. A PLL clock recovery which synchronizes to the clock source from the field generates the 13.56MHz clock to receiver and DBB.

The single-wire protocol (SWP) section provides the infrastructure to support up to 2 UICC cards and 1 microSD or secure element (SE).

The PMU section comprises of various low dropout regulators (LDOs) for power supply noise suppression and voltage regulation.

The Baseband section is the main controller to the RF, PMU and SWP section and also contains the MODEM, coding and decoding functions.

The power harvesting section enables MT6605 to perform card emulation during the absence of battery. The power will be harvested from the field.

3.2 Functional Block Diagram (Digital Part)

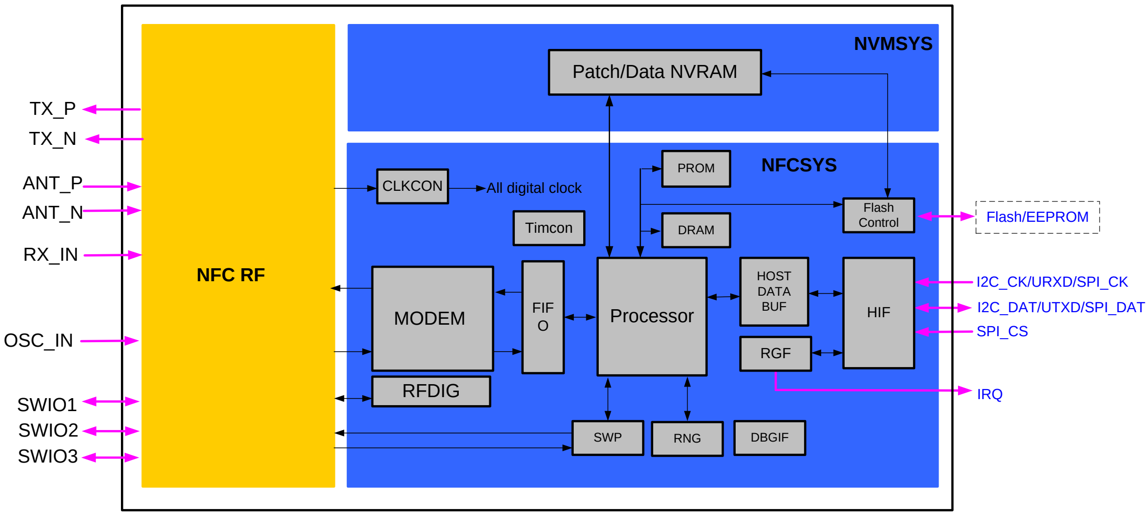

Figure 3-2: MT6605 digital block diagram

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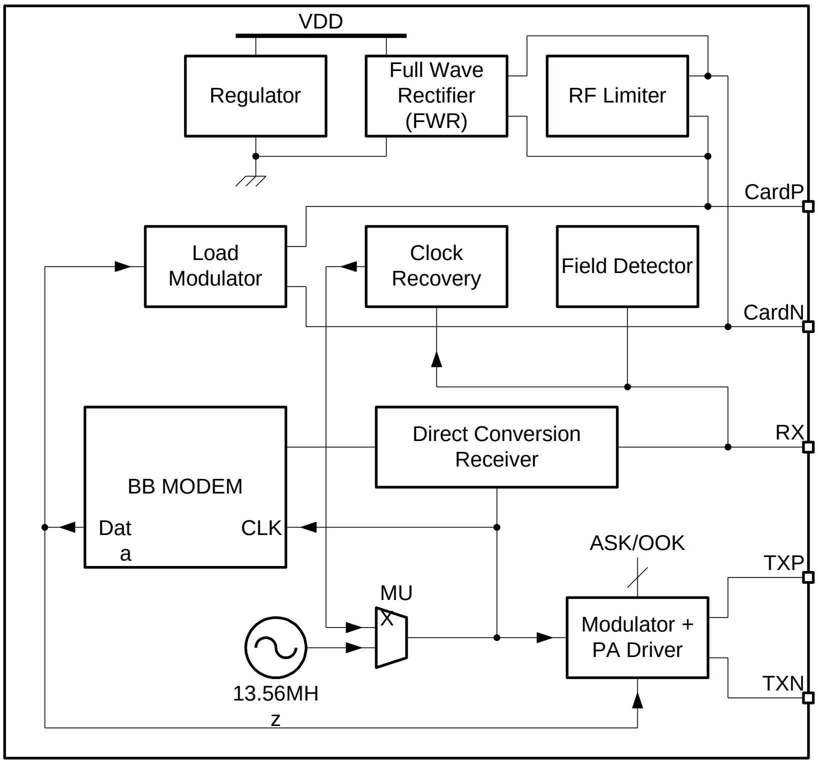
3.3 Functional Block Diagram (RF part)



During PCD mode, the PA Driver will transmit modulated signals and receive the load modulated signals from the PICC in the direct conversion receiver.
During PICC mode, clock is extracted from the field and recovered by the clock recovery circuit. TX is performed through load modulation at the CardP and CardN pins. The RF limiter circuit prevents the chip from “overharvesting field power” and regulates the voltage through shunting additional currents to ground.

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4 Package Description

4.1 Top mark

4.1.1 4X4 Package MCM with Serial Flash

MTK
MT6605N
DDDDDD
LLLLLL
• UUUUUU

N: QFN package
DDDDDD: Date code
LLLLLL: Die1 Lot number
UUUUUU: Die2 Lot number

4.1.2 4.5X4.5 Package MCM with Security Element

MTK
MT6605NS
DDDDDD
LLLLLL
• UUUUUU

N: QFN package
DDDDDD: Date code
LLLLLL: Die1 Lot number
UUUUUU: Die2 Lot number

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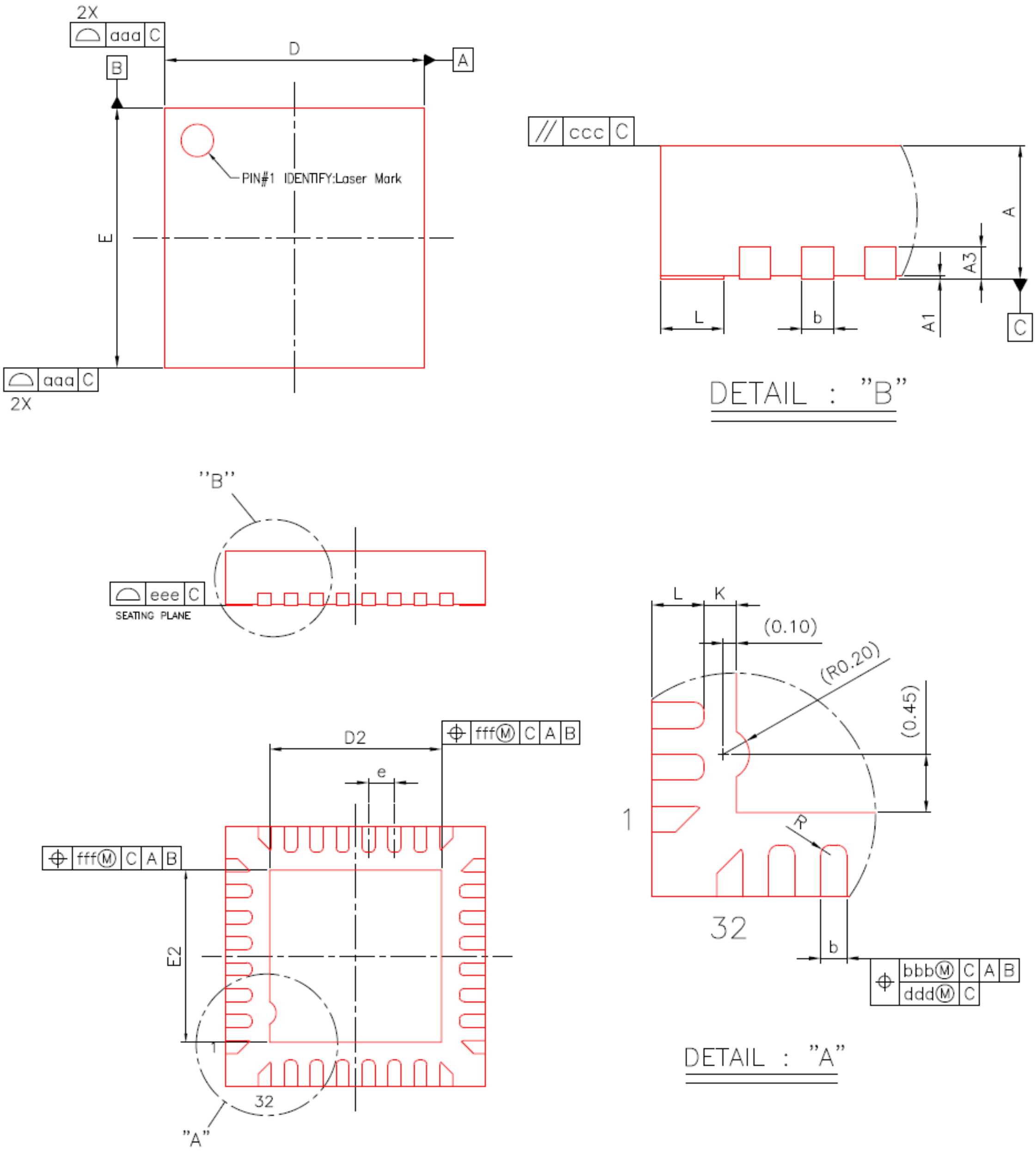
4.2 Package dimensions

4.2.1 4X4 Package dimensions



L/F	Exposed Pad Size						Internal Pad Size					
	Dimension in mm			Dimension in inch			Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
D2	2.50	2.65	2.80	0.098	0.104	0.110	2.75	2.90	3.05	0.108	0.114	0.120
E2	2.50	2.65	2.80	0.098	0.104	0.110	2.75	2.90	3.05	0.108	0.114	0.120

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Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.90	4.00	4.10	0.154	0.157	0.161
E	3.90	4.00	4.10	0.154	0.157	0.161
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.220	0.275	0.330	0.009	0.011	0.013
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

2. REFERENCE DOCUMENT: JEDEC MO-220.

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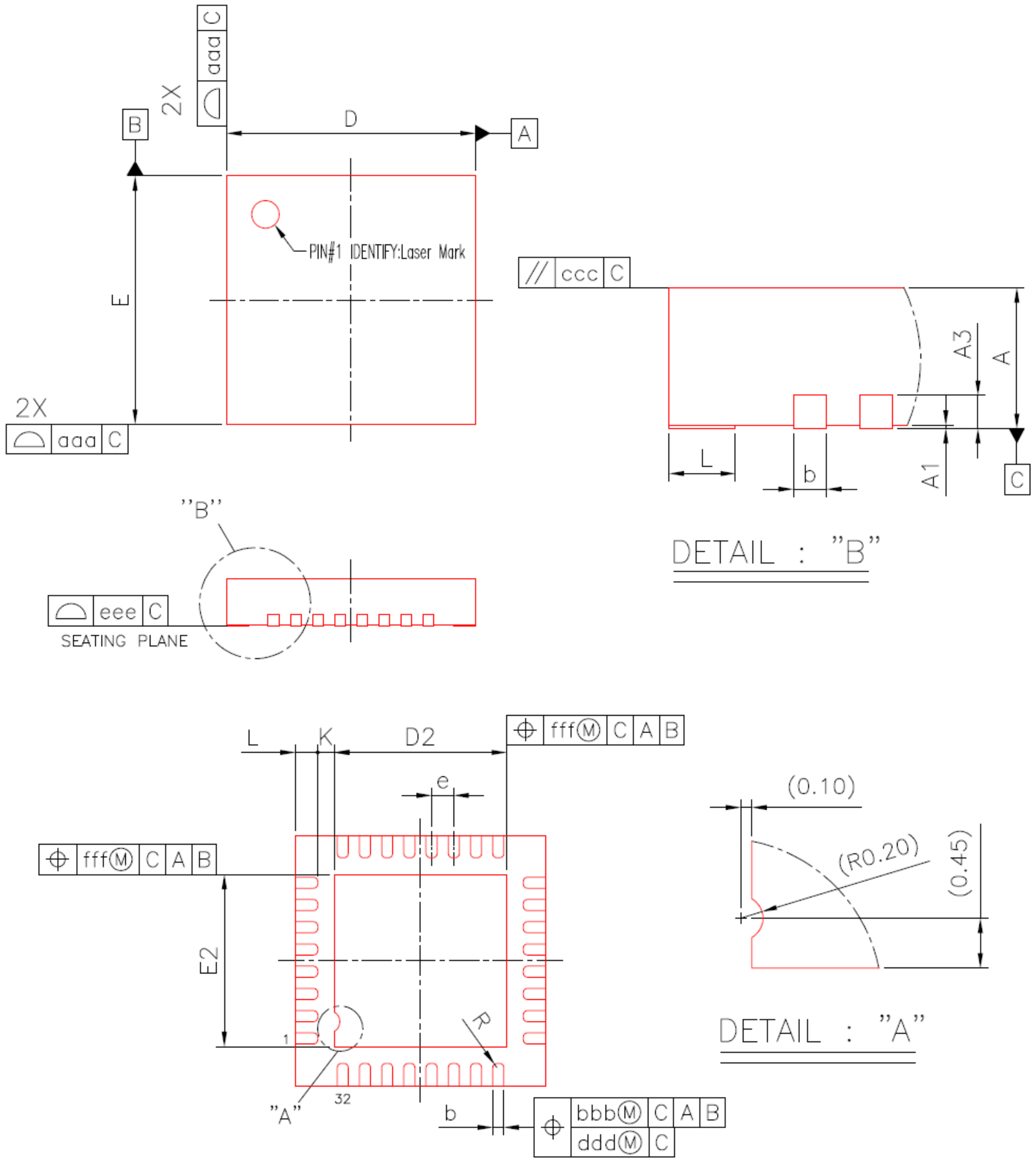
4.2.2 4.5X4.5 Package dimensions



L/F	Exposed Pad Size						Internal Pad Size					
	Dimension in mm			Dimension in inch			Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
D2	2.95	3.10	3.25	0.116	0.122	0.128	3.25	3.40	3.55	0.128	0.134	0.140
E2	2.95	3.10	3.25	0.116	0.122	0.128	3.25	3.40	3.55	0.128	0.134	0.140

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Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	4.40	4.50	4.60	0.173	0.177	0.181
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.24	0.30	0.36	0.009	0.012	0.014
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

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